## REMARKS/ARGUMENTS

Examiner:

Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which applicant regards as the invention.

Response:

Claims 1, 5, 10, and 17-19 have been amended as required by the Examiner to overcome this objection. No new material has been introduced. Reconsideration of claims 1-22 under 35 U.S.C. 112, second paragraph, is respectfully requested.

Examiner:

Claims 1, 10, and 17, as best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by the Scott et al. reference (U.S. Patent 6,369,661).

Response:

Claims 1, 10, and 17 have been amended to overcome this rejection. As amended, independent claims 1, 10, and 17 each comprise the limitation of utilizing a plurality of periods of a single reference clock to generate an output clock where a period of the

output clock is equal to a sum of the plurality of periods of the reference clock. No new material has been introduced.

Scott et al. selectively sums currents (Fig.9, Col.6, lines 56-65) and interpolates between a phase of a first summed signal and a phase of a second summed signal to generate a third signal (Abstract) to produce an output clock. Additionally, the switch Scott et al. uses to select which currents are summed prevents the reference from generating a plurality of output clocks simultaneously and cannot address the applications prior art problem of using a reduced number of inverters in the ring oscillator to reduce power consumption and improve stability. Merely adding a frequency divider to Scott et al. will not solve this problem.

On the other hand, the present invention does not selectively sum or interpolate currents, but utilizes the rising and/or falling edges of a plurality of periods of a single reference clock to trigger one rising or falling edge of the output clock and is claimed as such. As previously stated, the difference between selectively summing currents and the method of the present invention can be clearly seen by comparing the current application's Fig.2 with Fig.6a. By utilizing a plurality of reference clock periods to generate a single period of the output clock, the desired phase difference can be generated while achieving the stated goal of reducing instability and jitters found in prior art reference clocks by reducing the number of invertors in the ring oscillator (Page 22, Line 24 – Page 23, Line 23).

Therefore, the Applicant believes that the present application as currently claimed represents a new and useful device not taught or anticipated by known prior art and respectfully requests reconsideration and allowance of independent claims 1, 10, and 17.

Sincerely yours,

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